IT6633E-T

3-to-1 HDMI 1.3 Active Switch with EDID RAM

Preliminary Datasheet

ITE TECH. INC.

General Description

The IT6633 is a three-to-one HDMI v .1.3 active s witch that support s a sign alling rate of up to 2.25Gbps and the new Deep Color m odes. A one-port SINK systems such as flat-p anel TVs or LCD projectors could als o easily up grade to three-port by adding an IT 6633 at the front. By default the IT6633 operates in hardware mod e and source selectio n is done by controlling the pins S1 and S2. It also comes with a sof tware mode that allows the sys tem to con trol it via a two-line serial interface PCSCL/PCSDA.

As a active switch, the IT6633 equalizes incoming TM DS data with optimal q uality regardless of the incoming signal quality. The highly acclaimed equalization technology of ITE TECH. INC. provides for support of long or low-quality HDMI cables at even the highest s peeds. Input terminations of the TMDS inputs and output current levels are both programmable. In addition, the input terminations are disconnectable and hence significantly lower the system power consumption in inactive modes.

The IT6633 embeds an EDID RAM to save the cost of the three external EDID ROMs. The process of downloading the EDID dat a into the RAM is simplifi ed by the automatic read- back cap ability of the IT6633, minimizing the need of MCU interv ention. The IT6633 also embeds three 1K-ohm resisters for HPD signal paths to save external resisters and easy to implement the plug authentication.

The IT6633 also incorporates I^2C repeater in its DDC switches, which isolates the DDC capacitances of the two sides of the switch. This allows for longer cable cascading as well as significantly eases the system design to pass **Test ID 8-9: DDC/CEC Line Capacitance and Voltage** of the HDMI Compliance Test.

The IT6633 also distinguish itself from its peers in that it offers ±8kV of Human Body Mode ESD protection to all TMDS high-speed input pins. This saves significant costs in external high-speed ESD diodes, which could be very expensive .

Features

- HDMI active switch, providing superior performance over traditional passive switches
- Compliant with HDMI 1.3 and DVI 1.0 standards
- Serial data rate at up to 2.25Gbps, capable of supporting the following digital video formats in Deep Color Mode at up to 36 bits (12 bits/color):
  - DTV resolutions: 480i, 576i, 480p, 576p, 720p, 1080i to 1080p
  - PC resolutions: VGA, SVGA, XGA, SXGA to UXGA
- Single 3.3V operation
- Internal AC-coupling at TMDS inputs to cope with uneven intra-pair DC levels of incoming TMDS signals.
- Embedded EDID RAM saves external EDID ROM costs
- Embedded HDP resistors
- Integrated HPD switches
- Active port detection by monitoring TMDS input clock.
- DDC I^2C repeater isolates backend DDC capacitive loading from frontend, enhancing the DDC operation compatibility
- Human Body Mode ESD protection up to ±8kV for all TMDS differential input pins
- Disconnectable input terminations with auto-calibrated impedances
- Adaptive input equalization supporting long and short cables at the same time
- Default hardware-mode port selection and optional software-mode operation providing flexibility
- Programmable TMDS output current level
- Programmable source terminations compliant with HDMI 1.3 standard, providing optimal source data eyes at high speeds
- High-impedance TMDS output when disabled
- Optional backend receiver termination detection for auto powerdown
- 64-Pin LQFP package
- RoHS Compliant (100% Green available)

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6633E-T	0~70	64-pin LQFP	Green

Pin Diagram

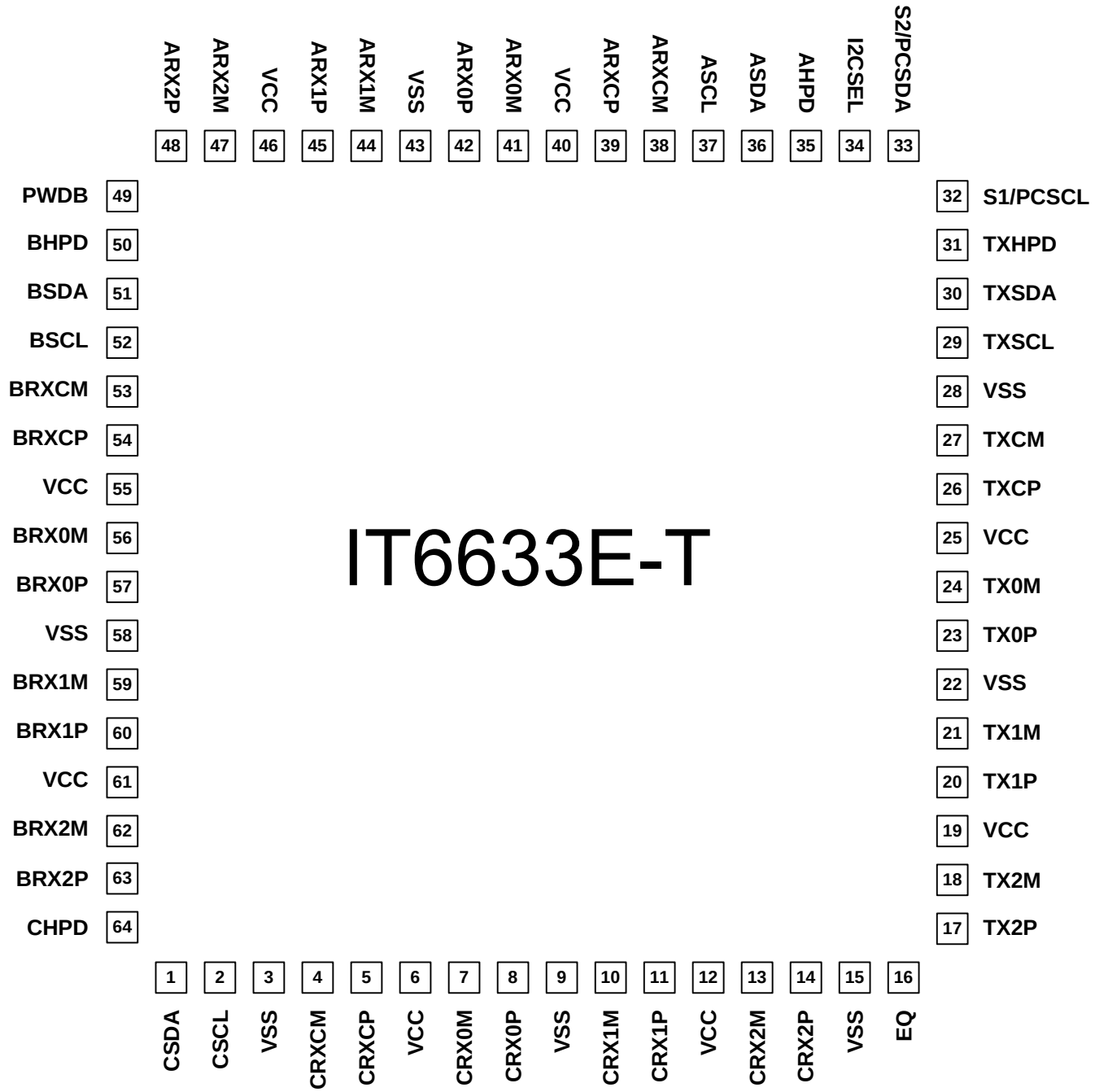


Figure 1. IT6633 pin diagram

Pin Description

TMDS High Speed Differential Input Pins (All these pins provide ±8kV HBM ESD Protection)

Pin Name	Direction	Description	Type	Pin No.
ARX2P	Input	Channel 2 positive input of Port A	TMDS	48
ARX2M	Input	Channel 2 negative input of Port A	TMDS	47
ARX1P	Input	Channel 1 positive input of Port A	TMDS	45
ARX1M	Input	Channel 1 negative input of Port A	TMDS	44
ARX0P	Input	Channel 0 positive input of Port A	TMDS	42
ARX0M	Input	Channel 0 negative input of Port A	TMDS	41
ARXCP	Input	Clock channel positive input of Port A	TMDS	39
ARXCM	Input	Clock channel negative input of Port A	TMDS	38
BRX2P	Input	Channel 2 positive input of Port B	TMDS	63
BRX2M	Input	Channel 2 negative input of Port B	TMDS	62
BRX1P	Input	Channel 1 positive input of Port B	TMDS	60
BRX1M	Input	Channel 1 negative input of Port B	TMDS	59
BRX0P	Input	Channel 0 positive input of Port B	TMDS	57
BRX0M	Input	Channel 0 negative input of Port B	TMDS	56
BRXCP	Input	Clock channel positive input of Port B	TMDS	54
BRXCM	Input	Clock channel negative input of Port B	TMDS	53
CRX2P	Input	Channel 2 positive input of Port C	TMDS	14
CRX2M	Input	Channel 2 negative input of Port C	TMDS	13
CRX1P	Input	Channel 1 positive input of Port C	TMDS	11
CRX1M	Input	Channel 1 negative input of Port C	TMDS	10
CRX0P	Input	Channel 0 positive input of Port C	TMDS	8
CRX0M	Input	Channel 0 negative input of Port C	TMDS	7
CRXCP	Input	Clock channel positive input of Port C	TMDS	5
CRXCM	Input	Clock channel negative input of Port C	TMDS	4

TMDS High Speed Differential Output Pins

Pin Name	Direction	Description	Type	Pin No.
TX2P	Output	Channel 2 positive output of output port	TMDS	17
TX2M	Output	Channel 2 negative output of output port	TMDS	18
TX1P	Output	Channel 1 positive output of output port	TMDS	20
TX1M	Output	Channel 1 negative output of output port	TMDS	21
TX0P	Output	Channel 0 positive output of output port	TMDS	23
TX0M	Output	Channel 0 negative output of output port	TMDS	24

TXCP	Output	Clock channel positive output of output port	TMDS	26
TXCM	Output	Clock channel negative output of output port	TMDS	27

DDC and HPD Control Pins

Pin Name	Direction	Description	Type	Pin No.
ASCL	I/O	Port A DDC bus clock line	5V-Tol.	37
ASDA	I/O	Port A DDC bus data line	5V-Tol.	36
BSCL	I/O	Port B DDC bus clock line	5V-Tol.	52
BSDA	I/O	Port B DDC bus data line	5V-Tol.	51
CSCL	I/O	Port C DDC bus clock line	5V-Tol.	2
CSDA	I/O	Port C DDC bus data line	5V-Tol.	1
TXSCL	I/O	Output Port DDC bus clock line	5V-Tol.	29
TXSDA	I/O	Output Port DDC bus data line	5V-Tol.	30
TXHPD	Input	HPD signal of the HDMI Sink	5V-Tol.	31
AHPD	Output	HPD signal to be sent back to Source connected to Port A	LVTTL	35
BHPD	Output	HPD signal to be sent back to Source connected to Port B	LVTTL	50
CHPD	Output	HPD signal to be sent back to Source connected to Port C	LVTTL	64

Other Control and Configuration Pins

Pin Name	Direction	Description	Type	Pin No.
EQ	Input	Control of equalization. ‘0’: long cable ‘1’: short cable	LVTTL	16
S1/PCSCL	Input	Port select/serial programming Clock for chip programming (5V-tolerant)	Schmitt	32
S2/PCSDA	I/O	Port select/serial programming Data for chip programming (5V-tolerant) GPIO mode: S[2:1] “00”: Input port C is selected “01”: Standby mode “10”: Input port B is selected “11”: Input port A is selected	Schmitt	33
I2CSEL	Input	GPIO/I2C select: ‘1’: GPIO ‘0’: I2C	LVTTL	34
PWDB	Input	Power down signal (low-active)	LVTTL	49

Power and Ground Pins

Pin Name	Description	Type	Pin No.
VCC	Chip power supply (3.3V)	Power	6, 12, 19, 25, 40, 46, 55, 61
VSS	Chip ground	Ground	3, 9, 15, 22, 28, 43, 58

Functional Description

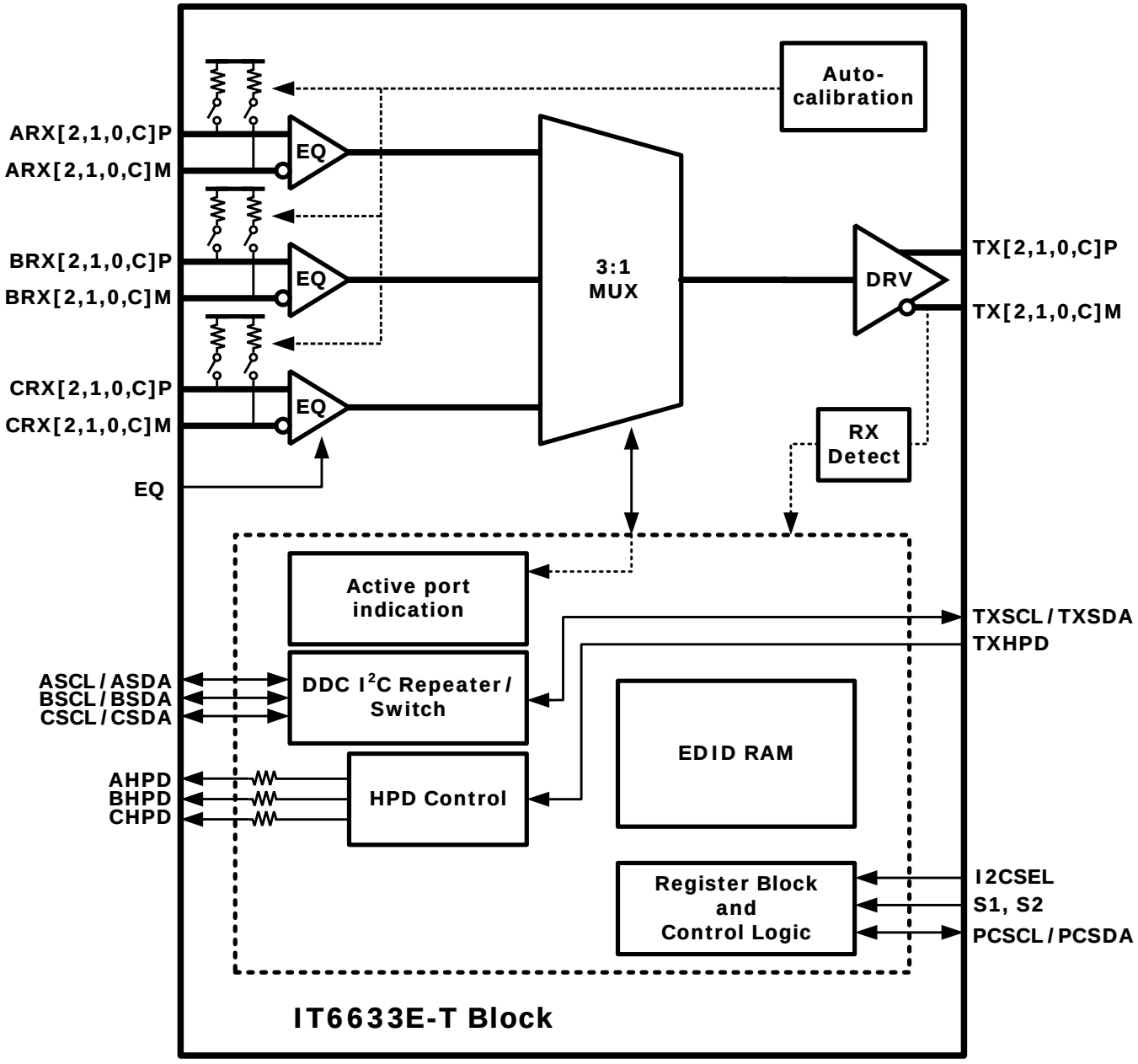


Figure 2. Functional block diagram of IT6633

Power Consumption

Conditions: Typ VCC=3.3V

- Operation Supply Current

Mode Condition		Current
1080P 12 bit	Typ	**180mA**

- S tandby Current

Standby T	yp	**11.5mA**

- Power Down Current

Power Down	Typ	**2.5mA**

Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter		Min.	Typ	Max	Unit
VCC Supply	voltage		-0.3		4.0	V
V_I Input	voltage		-0.3		VCC+0.3	V
V_O Output	voltage		-0.3		VCC+0.3	V
V_{IDDC}	DDC control pins input voltage		-0.3		6.0	V
T_J Junction	Temperature				125	°C
T_{STG} S	torage Temperature		-65		150	°C
ESD_HB	Human body mode	ARXs, BRXs, CRXs	8000			V
	ESD sensitivity	All other pins	2000			
ESD_MM	Machine mode ESD sensitivity		200			V

Notes:
1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.
2. Refer to Functional Operation Conditions for normal operation.

Functional Operation Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
V_{CC}	Supply voltage[1]	3.135	3.3	3.465	V
T_A	Ambient temperature	0	25	70	°C
Θ_{ja}	Junction to ambient thermal resistance			40	°C/W
TMDS Differential Pins					
V_{IDIFF}	TMDS differential input swing (peak-to-peak)	150		1560	mV
V_{TERM}	TMDS output termination voltage[1]	3.135	3.3	3.465	V
T_{bit}	Average bit time of the TMDS data stream	0.444		40	ns
R_{bit}	Signaling rate of the serial TMDS data stream	250		2250	Mbps
DDC I/O Pins (ASCL/ASDA, BSCL/BSDA, CSCL/CSDA and TXSCL/TXSDA)					
V_{IDDC}	DDC input voltage	0		5.5	V

Notes:
1. This is mandated by the HDMI Specifications v1.3 as the supply voltage at pin VCC is also the HDMI termination voltage.

DC Electrical Specification

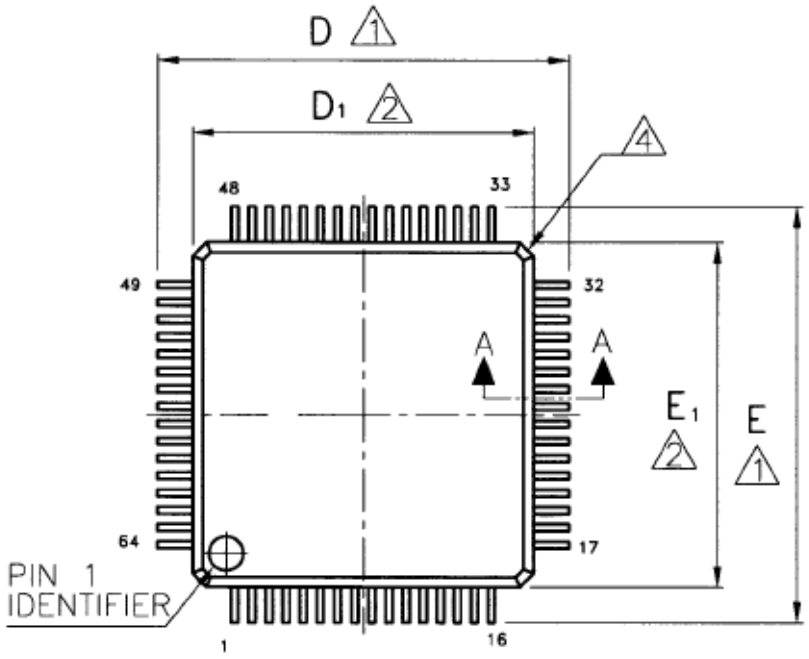
Under functional operation conditions

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
TMDS Differential Output Pins (TX2P/M, TX1P/M, TX0P/M, TXCP/M)						
V_{OHTMDS}	TMDS output high voltage[3]	R_{LOAD}=50Ω	V_{CC}-10		V_{CC}+10	mV
V_{OLTMDS}	TMDS output low voltage[3]	V_{CC}=V_{TERM}=3.3V	V_{CC}-700		V_{CC}-400	mV
V_{swing}	TMDS output single-ended swing[3]		400		600	mV
I_{OFF}	Single-ended standby output current[3]	V_{OUT}=0			10	μA
Logic I/O Pins (LVTTL and Schmitt)						
V_{IH}	Input high voltage[1]		2.0			V
V_{IL}	Input low voltage[1]				0.8	V
V_T Switching	threshold[1]			1.5		V
V_{OL}	Output low voltage[1]	I_{OL}=2~16mA			0.4	V
V_{OH}	Output high voltage[1]	I_{OH}=-2~-16mA 2.4				V
V_{T-}	Schmitt trigger negative going threshold voltage[1]	0.8		1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage[1]			1.6	2.0	V
I_{IN}	Input leakage current[1]	V_{IN}=5.5V or 0		±5		μA
I_{OZ}	Tri-state output leakage current[1]	V_{IN}=5.5V or 0		±10		μA
I_{OL}	Serial programming output sink current[2]	V_{OUT}=0.2V 4			16	mA

Notes:

1. Guaranteed by I/O design.
2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.2V. In a real serial programming environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I^2C Standard. When set at maximum current, the serial programming output ports of IT6633E are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I^2C V_{IL}. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to the IT6633E Register Table for proper register setting.
3. Limits defined by HDMI 1.3 standard

Package Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

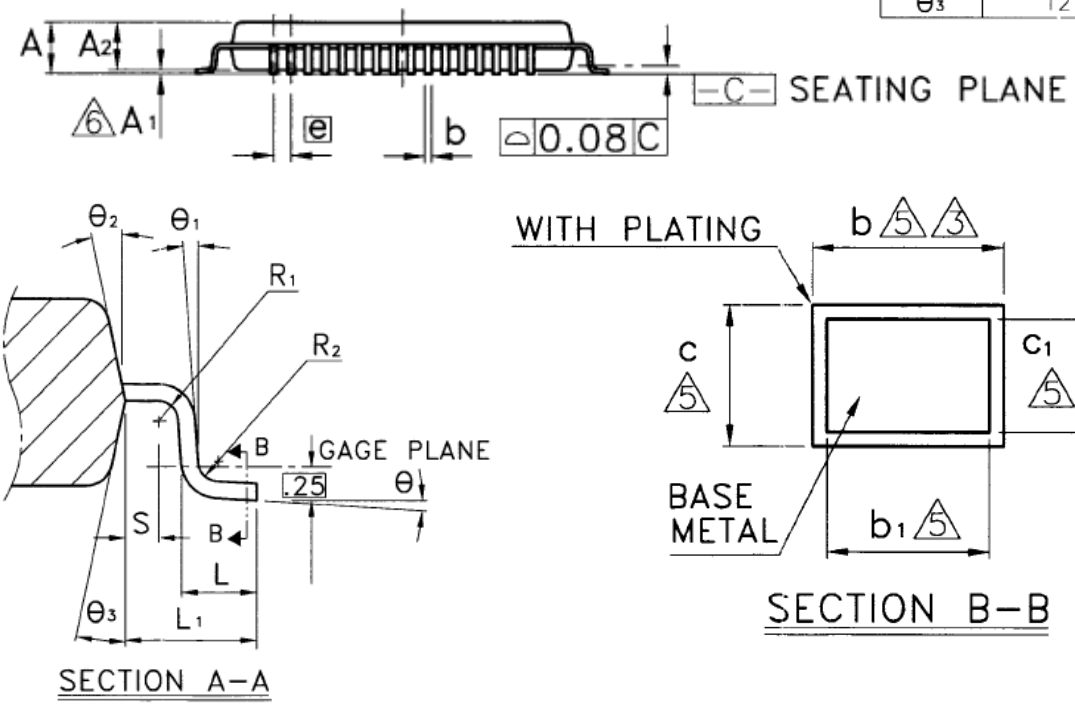


Figure 3. 64-pin LQFP Package Dimensions